CLAIMS

What is claimed is:

1. A buffer, comprising:

a current source coupled to provide a current signal substantially independent of temperature variations;

a bias circuit adapted to provide a first bias signal in response to the current signal;

a decoupler, responsive to the first bias signal and a first power supply signal, and adapted to provide a load signal that is independent of noise present in the first power signal; and

an input stage coupled to receive the load signal as its supply reference, and adapted to provide an output signal that is independent of the noise in the first power signal and the temperature variations.

2. The buffer according to Claim 1, wherein the current source comprises:

an inversely Proportional To Absolute Temperature (PTAT) element coupled to provide a decreasing PTAT current signal with increasing temperature; and

a PTAT element coupled to receive the decreasing PTAT current signal and arranged to provide an increasing PTAT voltage signal with increasing temperature.

3. The buffer according to Claim 2, wherein the current source further comprises a startup circuit adapted to provide a first current path prior to steady state operation of the buffer and a second current path subsequent to steady state operation of the buffer.

4. The buffer according to Claim 1, wherein the bias circuit comprises a first current conduction device coupled to receive the current signal at a first node and coupled to provide the first bias signal at the first node.

5. The buffer according to Claim 4, wherein the decoupler comprises a second current conduction device having a geometry in ratio proportion to the first current conduction device.

6. The buffer according to Claim 5, wherein the second current conduction device includes a P-type Field Effect transistor having a source terminal coupled to receive the first power supply signal and a drain terminal coupled to provide the load signal.

7. The buffer according to Claim 1, wherein the input stage comprises a differential transistor pair having conductors coupled to receive the load signal at a second node.

8. The buffer according to Claim 7, wherein the differential transistor pair includes first and second P-type Field Effect transistors having a first drain terminal coupled to provide the output signal in response to a first phase of the input signal and a second drain terminal coupled to provide the output signal in response to a second phase of the input signal.

9. The buffer according to Claim 8, further comprising active loads coupled to the first and second drain terminals, wherein a conductivity state of the active loads is referenced to a second bias signal generated in proportion to the current signal.

10. The buffer according to Claim 9, further comprising a clamp circuit coupled to the active loads to prevent the output signal from exceeding a predetermined value, wherein a conductivity state of the clamp circuit is referenced to a third bias signal generated in proportion to the current signal.

11. The buffer according to Claim 9, further comprising a cross-coupled circuit coupled to the active loads and the input stage to accelerate transitions of the output signal.

12. The buffer according to Claim 11, wherein the cross-coupled circuit comprises:

a first N-type Field Effect transistor having a control terminal coupled to the second drain terminal and a first conductor coupled to the first drain terminal; and

a second N-type Field Effect transistor having a control terminal coupled to the first drain terminal and a first conductor coupled to the second drain terminal.

13. A buffer circuit, comprising:

means for providing a current signal substantially independent of temperature variations;

means for providing a first bias signal in response to the current signal;

means, responsive to the first bias signal and a first power supply signal, for providing a load signal that is independent of noise present in the first power signal; and

means, coupled to receive the load signal as its supply reference, for providing an output signal that is independent of the noise in the first power signal and the temperature variations.

14. The buffer circuit according to Claim 13, further comprising means for clamping the output signal to a predetermined level.

15. The buffer circuit according to claim 14, further comprising means for accelerating transitions of the output signal.

16. A buffer adapted to operate substantially independently of temperature variations, and of power-supply, noise-induced jitter, the buffer comprising:

a current generator adapted to generate a current bias substantially independent of temperature variation;

a bias generator coupled to receive the current bias and coupled to the first power supply to produce a bias signal;

a decoupler coupled to receive the bias signal, wherein the bias signal renders a conductivity state of the decoupler to provide a load signal that is substantially independent of a first power supply level variation due to noise;

a differential transistor pair coupled to receive first and second inputs and the load signal, wherein the load signal is conducted by the differential transistor pair in response to the first and second inputs; and

a load circuit coupled to the differential transistor pair and coupled to provide a differential output signal at first and second nodes, the load circuit including:

a cross coupled circuit coupled to the first and second nodes, wherein the cross coupled circuit decreases a negative transition time of the output signal at the first node in response to an increased conductivity state of the cross coupled circuit caused by the output signal at the second node.